REMARKS

In response to the action of August 14, 2007, applicants asks that all claims be allowed in view of the amendments to the claims and the following remarks.

Claims 1-17, 19-36 and 38-44 are currently pending, of which claims 1, 2, 13, 20, 21 and 32 are independent. Claims 1, 2, 13, 14, 20, 21 and 32 have been amended. Support for these amendments may be found in the application at, for example, page 17, lines 29-36; page 18, lines 14-16; and page 26, lines 6-11. No new matter has been introduced.

Non-Statutory Double Patenting Rejections

Claims 1-17, 19-36 and 38-44 are rejected as obvious over claims 1-28 of U.S. Patent No. 7,027,074 in view of Nishoioka (U.S. Patent No. 5,390,293) and Kuwajima (U.S. Patent No. 6, 339,422). Claims 1, 2, 13, 20, 21 and 32 have been amended to recite that the display and the display controller are formed over a common substrate. Claims 1, 2, 13 have been amended to recite that the second means has a lower voltage for driving the source signal line driver circuit and the gate signal line driver circuit than the first means, and claims 20, 21 and 32 have been amended to recite that the second display mode has a lower voltage for driving the source signal line driver circuit and the gate signal line driver circuit than the first display mode. These features are not described or suggested by the claims of U.S. Patent No. 7,027,074, or by Nishoioka or Kuwajima, alone or in any proper combination. Nor does the action assert that these features are described or suggested by the applied references. For example, although the action contends that Kuwajima discloses a voltage applied to the pixel element, Kuwajima does not describe or suggest a second display mode (or a second means) that has a lower voltage for driving the source signal line driver circuit and the gate signal line driver circuit than the first display mode (or a first means), as recited by claims 1, 2, 13, 20, 21 and 32. See action at page 3 (stating "Kuwajima et al teach a voltage applied to the pixel element...." and citing figs. 2-3, col. 7, lines 66-68; col. 8, lines 1-6). Accordingly, applicant requests reconsideration and withdrawal of this rejection.

Claims 1-17, 19-36 and 38-44 are provisionally rejected as obvious over claims 1-26 of copending Application No. 10/385,712, now allowed, in view of Nishioka and Kuwajima. As noted above, claims 1, 2, 13, 20, 21 and 32 have been amended to recite features not described or suggested by Nishioka or Kuwajima. Nor do the claims of Application No. 10/385,712 recite that the display and the display controller are formed over the common substrate, the second means has a lower voltage for driving the source signal line driver circuit and the gate signal line driver circuit than the first means, or the second display mode has a lower voltage for driving the source signal line driver circuit and the gate signal line driver circuit than the first display mode. Accordingly, applicant requests reconsideration and withdrawal of this rejection.

Claims 1-17, 19-36 and 38-44 are provisionally rejected as obvious over claims 1-27 of copending Application No. 11/419,345, now allowed, in view of Nishioka. As noted above, claims 1, 2, 13, 20, 21 and 32 have been amended to recite features not described or suggested by Nishioka. Nor do the claims of Application No. 11/419,345 recite that the display and the display controller are formed over a common substrate, the second means has a lower voltage for driving the source signal line driver circuit and the gate signal line driver circuit than the first means, and the second display mode has a lower voltage for driving the source signal line driver circuit and the gate signal line driver circuit than the first display mode. Accordingly, applicant requests reconsideration and withdrawal of this rejection.

Rejection of Claims 1-8, 11-16, 19-27, 30-35 and 38-44

Claims 1-8, 11-16, 19-27, 30-35 and 38-44 have been rejected as being unpatentable over Koyama (U.S. Publication No. 2002-0154151) in view of Nishioka. Applicant requests reconsideration and withdrawal of the rejection because neither Koyama, Nishioka nor any proper combination of the references describes or suggests the subject matter of independent claims 1, 2, 13, 20, 21 and 32.

Independent Claims 1, 2 and 13 and Dependent Claims 3-8, 11, 12, 14-16, 19 and 39-41

Claim 1 recites a display device that includes a display controller and a display including a source signal line driver circuit and a gate signal line driver circuit. The display device also

includes a first means that divides one frame period into subframe periods, sets one of lighting and non-lighting to each of the subframe periods, and expresses n-bits gradation (where n is a natural number of two or more) in accordance with a total lighting time during the one frame period. The display device also includes a second means that does not divide one frame period into subframe periods, that sets one of lighting and non-lighting to the one frame period, that expresses 1-bit gradation in accordance with a total lighting time during the one frame period. The display controller controls the first means and the second means. The display and the display controller are formed over a common substrate. Each of independent claims 2 and 13 recites similar features.

Neither Koyama, Nishioka, nor any proper combination of the two describes or suggests many of the features recited in each of amended independent claims 1, 2 and 13. For example, neither Koyama, Nishioka, nor any proper combination of the references describes or suggests that the display and the display controller are formed over a common substrate, or that the second means has a lower voltage for driving the source signal line driver circuit and the gate signal line driver circuit than the first means, as recited by each of independent claims 1, 2 and 13.

The action relies on Koyama for disclosing a display and a display controller. See action at page 7 (indicating Koyama discloses "a display; a display controller (102)" and citing Fig. 4 and paragraph 227). Koyama discloses a "display device that is structured by a signal control circuit 101, a display controller 102, and a display 100." See Koyama at paragraph 227. Koyama's Figures 4 and 6 show a block diagram of the display device. See Koyama at paragraph 226. Koyama's "display controller 102 is structured by a standard clock generator circuit 301, a variable frequency divider circuit 302, a horizontal clock generator circuit 303, a vertical clock generator circuit 304, and an electric power source 305 used for the light emitting elements," which is shown in Figures 3 and 4. See Koyama at paragraph 242; see also Koyama at paragraphs 226 and 227. Koyama nowhere indicates that the display and the display controller are formed over a common substrate, as recited in amended claims 1, 2 and 13.

Nishioka discloses "a display unit, such as an LCD (liquid crystal display), [sic] 23 which can present a multicolor display...." See Nishioka at col. 7, lines 18-20. Nishioka also discloses "a display control circuit 80 shown in FIG. 11 [that] includes a display controller 93...." See Nishioka at col. 16, lines 40-41. Nishioka nowhere indicates that the display and the display controller are formed over a common substrate, as recited in amended claims 1, 2 and 13.

Accordingly, neither Koyama, Nishioka, nor any proper combination of the references describes or suggests that the display and the display controller are formed over a common substrate, as recited in amended claims 1, 2 and 13.

In addition, neither Koyama, Nishioka, nor any proper combination of the references describes or suggests that the second means has a lower voltage for driving the source signal line driver circuit and the gate signal line driver circuit than the first means, as recited by each of independent claims 1, 2 and 13. Although Koyama discloses, in paragraph 262, that the "voltage applied between both the electrodes of the light emitting element can be made smaller in the second display mode," Koyama does not describe or suggest a second means not for dividing one frame period into a plurality of subframe periods, for setting one of lighting and non-lighting to the one frame period, and for expressing 1-bit gradation in accordance with a total lighting time during the one frame period, where the second means has a lower voltage for driving the source signal line driver circuit and the gate signal line driver circuit than the first means, as recited by amended claims 1, 2 and 13.

Nishoka discloses power reserving techniques that include a battery in which the terminal voltage lowers with decrease in the power reserve. See col. 21, lines 18-60. Nishoka does not describe or suggest that the second means has a lower voltage for driving the source signal line driver circuit and the gate signal line driver circuit than the first means, as recited by amended claims 1, 2 and 13.

Therefore, neither Koyama, Nishioka, nor any proper combination of the references describes or suggests that the second means has a lower voltage for driving the source signal line driver circuit and the gate signal line driver circuit than the first means, as recited by amended claims 1, 2 and 13.

Accordingly, for at least these reasons, applicant requests reconsideration and withdrawal of the rejection of independent claims 1, 2 and 13 and their respective dependent claims 3-8, 11, 12, 14-16, 19 and 39-41.

Independent Claims 20, 21 and 32 and Dependent Claims 22-27, 30, 31, 33-35, 38 and 42-44

Claim 20 recites, among other elements, a display including a source signal line driver circuit and a gate signal line driver circuit and a display controller, and a first and second display modes, where the display and the display controller are formed over a common substrate and the second display mode has a lower voltage for driving the source signal line driver circuit and the gate signal line driver circuit than the first display mode. Each of claims 21 and 32 recites similar features.

As described above with respect to claims 1, 2 and 13, neither Koyama, Nishioka, nor any proper combination of the references describes or suggests that the display and the display controller are formed over a common substrate, which also is recited by amended claims 20, 21 and 32.

Also, for reasons similar to those discussed above with respect to claims 1, 2 and 13, neither Koyama, Nishioka, nor any proper combination of the references describes or suggests that the second display mode has a lower voltage for driving the source signal line driver circuit and the gate signal line driver circuit than the first display mode, as recited in claims 20, 21 and 32.

For at least these reasons, applicant respectfully requests reconsideration and withdrawal of the rejection of independent claim 20, 21 and 32 and their respective dependent claims 22-27, 30, 31, 33-35, 38 and 42-44.

Rejection of Claims 9, 10, 17, 28, 29 and 36

Claims 9, 10, 17, 28, 29 and 36, which each depend from one of independent claims 1, 2, 13, 20, 21 and 32, respectively, have been rejected as being unpatentable over Koyama in view of Nishioka and Okuda (U.S. Patent No. 6,380,689). Okuda, which is cited in the action for disclosing a frame period comprising three periods of an address period, an emission period, and

a reset period, does not remedy the failure of Tanabe and Yamada to describe or suggest the subject matter of the independent claims. Accordingly, applicant respectfully requests reconsideration and withdrawal of the rejections of claims 9, 10, 17, 28, 29 and 36.

Conclusion

Applicant submits all claims are in condition for allowance.

It is believed that all of the pending issues have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this reply should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this reply, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

The fee in the amount of $120 in payment of a one-month extension of time fee is being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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